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## Seventh Semester B.E. Degree Examination, June/July 2019 Advanced Computer Architectures

Time: 3 hrs.

Max. Marks: 80

**Note: Answer any FIVE full questions, choosing ONE full question from each module.**

### Module-1

- 1 a. Explain the evolution of computer architecture. (08 Marks)
- b. Explain with diagram the operational model of SIMD super computer. (08 Marks)

OR

- 2 a. Explain the Bernstein's conditions for parallelism. Detect the parallelism in the following code using Bernstein's conditions. (Assume no pipeline).  
 $P_1 : C = D \times E$ ;  $P_2 : M = G + C$ ;  $P_3 : A = B + C$ ;  $P_4 : C = L + M$ ;  $P_5 : G \div E$ . (08 Marks)
- b. With a diagram, explain the operation of tagged token data flow computer. (08 Marks)

### Module-2

- 3 a. Distinguish between typical RISC and CISC process architectures. (08 Marks)
- b. With a diagrams, explain the models of a basic scalar computer system. (08 Marks)

OR

- 4 a. With a diagram, explain a typical superscalar RISC processor architecture consisting of an integer unit and a floating point unit. (10 Marks)
- b. With a diagram, explain the hierarchical memory technology. (06 Marks)

### Module-3

- 5 a. Explain with diagram, the backplane bus specification. (08 Marks)
- b. With the diagrams, explain the central arbitration and distribution arbitration. (08 Marks)

OR

- 6 a. For the reservation table of a non-linear pipeline shown below :

	1	2	3	4	5	6
S <sub>1</sub>	X					X
S <sub>2</sub>		X			X	
S <sub>3</sub>			X			
S <sub>4</sub>				X		
S <sub>5</sub>		X				X

- i) What are the forbidden latencies? Write initial collision vector
  - ii) Draw the state transition diagram
  - iii) List all simple cycles and greedy cycles
  - iv) Determine MAL. (10 Marks)
- b. Explain prefetch buffer and internal data forwarding mechanisms used in instruction pipelining. (06 Marks)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.  
2. Any revealing of identification, appeal to evaluator and/or equations written e.g. 42+8 = 50, will be treated as malpractice.

**Module-4**

- 7 a. Explain crossbar networks and cross-point switch design in multiprocessor system. (08 Marks)  
b. With necessary sketches, explain the cache-coherence problems in data sharing and in process migration. (08 Marks)

OR

- 8 a. With a diagram, explain the architecture of the connection machine CM-2. (08 Marks)  
b. Explain the context-switching policies. (08 Marks)

**Module-5**

- 9 a. Explain the concurrent OOP and an actor model in object – oriented model. (08 Marks)  
b. Explain the fairness policies and sole-access –protocols in the principles of synchronization. (08 Marks)

OR

- 10 a. What are the major hurdles of pipelining? Illustrate the branch hazards in detail. (08 Marks)  
b. Explain the dynamic scheduling of a pipeline using Tomasulo's algorithm. (08 Marks)

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